introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask,

wherein said step of introducing N atoms into said gate oxide film comprises a thermal annealing process of said gate oxide film conducted in an atmosphere containing NO,

said thermal annealing process being conducted at a temperature of about 800°C.

10. (Three Times Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask,

wherein said step of introducing N atoms into said gate oxide film comprises the steps of conducting an ion implantation process of N ions; and applying a thermal annealing process to said gate oxide film.

13. (Amended) A method as claimed in claim 6, further comprising the step of forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing impurity elements into said substrate through said gate oxide film while using said gate electrode pattern as a mask, and wherein said step of introducing impurity elements is conducted prior to said step of introducing N atoms into said gate oxide film.

Please add new claims 15 and 16 as follows:

15. A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask, said step of introducing N atoms being conducted in an atmosphere containing NO; and

depositing, after said step of introducing N atoms, a CVD-oxide film on said gate oxide film by a CVD process,

wherein said step of introducing N atoms and said step of depositing said CVD-oxide film are conducted consecutively in a common processing chamber, without taking out said substrate into an atmospheric environment.

16. A method as claimed in claim 15, further comprising the step of forming diffusion regions at both lateral sides of said gate electrode pattern by introducing impurity elements into said substrate through said gate oxide film while using said gate electrode pattern as a mask, and wherein said step of introducing impurity elements is conducted prior to said step of introducing N atoms into said gate oxide film.